Applic. No.: 10/034,070
Amdt. Dated June 27, 2005
Reply to Office action of March 25, 2005

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-10, 12-21, and 23 are now in the application. Claims 1 and 12 have been amended. Claim 23 has been added. Claims 10 and 22 have been previously cancelled.

In item 3 on pages 2-6 of the above-mentioned Office action, claims 1, 4-10, 12, and 15-21 have been rejected as being unpatentable over Dreibelbis et al. ("Processor-Based Built-In Self-Test for Embedded DRAM," IEEE Journal of Solid State Circuits, Vol. 33 No. 11, November, 1998, pp1731-1740) in view of Wong (US 6,363,008) under 35 U.S.C. § 103(a).

In item 4 on pages 6-7 of the above-mentioned Office action, claims 2-3 and 13-14 have been rejected as being unpatentable over Dreibelbis et al. in view of Wong and further in view of Tsukakoshi et al. (US 5,337,318) under 35 U.S.C. § 103(a).

The rejections have been noted and claims 1 and 12 have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found, for example, on page 8, lines 5-16 of the specification.

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Before discussing the prior art in detail, it is believed that

a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

said setting memory being only accessible via said
registers of said buffer memory, said buffer memory being
used as latches for reading out and writing into said
setting memory.

Claim 12 calls for, inter alia:

connecting the setting memory to the buffer memory, the
setting memory being only accessible via the registers of
the buffer memory, the buffer memory being used as
latches for reading out and writing into the setting
memory.

None of the cited references discloses that the setting memory

is only accessible via the registers of the buffer memory and

that the registers of the buffer memory are used as latches

for reading out and writing into the setting memory, as

recited in claims 1 and 12 of the instant application.

It is accordingly believed to be clear that none of the

references, whether taken alone or in any combination, either

show or suggest the features of claims 1 and 12. Claims 1 and

12 are, therefore, believed to be patentable over the art and

since all the dependent claims are ultimately dependent on

claims 1 or 12, they are believed to be patentable as well.

New claim 23 has been added. Claim 23 includes the subject
matter of original claim 9. Claim 23 recites that the shift
register has at least one switch subdividing the shift
register into registers for the data processing unit. The
switch is arranged between the shift registers. This is
neither disclosed in Dreibelbis et al. nor any other cited
document.

The Examiner has stated that, regarding the subject matter of
claim 9, the registers in Dreibelbis et al. are switchable
under control of Row or Databit Commit (FIG. 6(a)). However,
this merely provides the function of selecting one or both of
the registers but does not selectively combine the registers
to an enlarged single shift register as is clearly disclosed
in Fig. 1 and the corresponding description in the
specification of the instant application.

Claim 23 is, therefore, believed to be patentable over the
art.

In view of the foregoing, reconsideration and allowance of
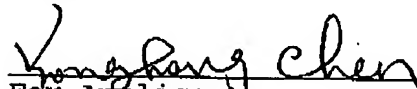claims 1-10, 12-21, and 23 are solicited.

In the event the Examiner should still find any of the claims
to be unpatentable, counsel would appreciate a telephone call

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so that, if possible, patentable language can be worked out.

In the alternative, the entry of the amendment is requested as

it is believed to place the application in better condition

for appeal, without requiring extension of the field of

search.

If an extension of time for this paper is required, petition

for extension is herewith made. Please charge any fees which

might be due with respect to 37 CFR Sections 1.16 and 1.17 to

the Deposit Account of Lerner and Greenberg, P.A., No. 12-

1099.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150

For Applicants

YC

June 27, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

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